AMENDMENTS TO THE CLAIMS:

Claim 1. (Currently amended) A state saving circuit comprising:

a first latch capable of performing a desired operation;

a second latch capable of saving the state of the first latch and of restoring the state of the first latch upon the powering up of the first latch, the second latch being powered by a power supply, wherein a ~~an integrated~~ control signal determines whether said second latch is in one of a state saving mode and a state restoring mode.

Claim 2. (Currently amended) The state saving circuit of claim 1,

wherein said power supply comprises an un-interruptible power supply; and

further comprising a cut-off control device powered by the un-interruptible power supply that selectively connects the second latch to a pair of latch nodes based upon said ~~integrated~~ control signal.

Claim 3. (Currently amended) A state saving circuit comprising:

a state saving latch powered by an un-interruptible power supply; and

a cut-off control device powered by the un-interruptible power supply that selectively connects the state saving latch to a pair of latch nodes based upon a ~~an integrated~~ control signal, wherein the ~~integrated~~ control signal determines whether said state-saving latch is in one of a state saving mode and a state restoring mode.

Claim 4. (Previously presented) The state saving circuit of claim 3, wherein said state saving latch comprises a pair of cross coupled inverters.

Claim 5. (Original) The state saving circuit of claim 4, wherein the pair of cross coupled inverters comprise a pair of CMOS inverters.

Claim 6. (Canceled).

Claim 7. (Currently amended) The state saving circuit of claim 3, wherein said cut-off control device disconnects the state saving latch from the pair of latch nodes when the ~~integrated~~ control signal has a predetermined low value.

Claim 8. (Original) The state saving circuit of claim 3, wherein said cut-off control device comprises a CMOS inverter.

Claim 9. (Canceled).

Claim 10. (Original) The state saving circuit of claim 8, wherein said cut-off control device further comprises a pair of transistors each having a gate in communication with an output of the CMOS inverter.

Claim 11. (Original) The state saving circuit of claim 3, wherein said state saving latch comprises a CMOS inverter.

Claim 12. (Original) The state saving circuit of claim 3, wherein the latch nodes comprise a true latch node and a complement latch node.

Claim 13. (Currently amended) The state saving circuit of claim 3, wherein the cut-off control device comprises:

an inverter receiving said ~~integrated~~ control signal, that inverts said ~~integrated~~ control signal and provides said ~~integrated~~ inverted control signal to gates of a first pair of transistors; and

a second pair of transistors receiving said ~~integrated~~ control signal at the gates of said second pair of transistors.

Claim 14. (Original) The state saving circuit of claim 13, wherein said latch nodes comprise a true node and a complement node.

Claim 15. (Original) The state saving circuit of claim 14, wherein one of said first pair of transistors is connected to said true node and the other of said first pair of transistors is connected to said complement node.

Claim 16. (Original) The state saving circuit of claim 13, wherein said state saving latch comprises a pair of cross coupled inverters.

Claim 17. (Original) The state saving circuit of claim 16, further comprising a third pair of transistors selectively connecting said first pair of transistors to a ground based upon input gate signals from said pair of cross-coupled inverters.

Claim 18. (Currently amended) The state saving circuit of claim 16, further comprising a third pair of transistors selectively connecting said second pair of transistors to a ground based upon input gate signals from ~~a~~ said pair of cross-coupled inverters.

Claim 19. (Currently amended) A circuit, comprising:

a D flip flop powered by an interruptible power supply and comprising a pair of latch nodes;

a state saving latch powered by an un-interruptible power supply; and

a cut-off control device powered by the un-interruptible power supply that selectively connects the state saving latch to said pair of latch nodes based upon a ~~an integrated~~ control signal,

wherein the ~~integrated~~ control signal determines whether said state-saving latch is in one of a state saving mode for enabling said state saving latch to follow a state of said D flip flop and a state restoring mode for restoring the state of said D flip flop from said state saving latch.

Claim 20. (Currently amended) A circuit, comprising:

an application specific integrated circuit powered by an interruptible power supply and comprising a pair of latch nodes;

a state saving latch powered by an un-interruptible power supply; and

a cut-off control device powered by the un-interruptible power supply that selectively connects the state saving latch to said pair of latch nodes based upon a ~~an integrated~~ control signal,

wherein the ~~integrated~~ control signal determines whether said state-saving latch is in one of a state saving mode for enabling said state saving latch to follow a state of said application specific integrated circuit and a state restoring mode for restoring the state of said application specific integrated circuit from said state saving latch.

Claim 21. (Currently amended) The circuit of claim 1, further comprising a cut-off control device powered by the un-interruptible power supply that selectively connects the second latch to a pair of latch nodes based upon said ~~integrated~~ control signal.

Claim 22. (Previously presented) The circuit of claim 1, wherein the second latch comprises a pair of cross coupled inverters.